

# ICS05

Sponsored by ACM/SIGARCH

## ICS05 Program

### Sunday, June 19, 2005

**6:30-8:00 pm Welcome Reception and Registration**  
(to be held at the Cambridge Marriott)

### Monday, June 20, 2005

**8:30 am** Welcome (Opening Remarks)

**8:40 am** Keynote  
**Burton Smith** (Cray, Inc.)  
Improving the State of Parallel Programming

#### 9:40 am Coffee Break

#### Session 1: Cache

**9:50 am** Reducing Latencies of Pipelined Cache  
Accesses Through Set Prediction  
*A. Aggarwal (Binghamton University)*

**10:10 am** Characterization of Private and Shared L3  
Cache Behavior of SPECjAppServer2002 and TPC  
*E. Nurvitadhi, N. Chalainanont, S. Lu  
(CMU, OSU, SLL-MRL, Intel Labs)*

**10:30 am** A Hybrid Hardware/Software Approach to  
Efficiently Determine Cache Coherence Bottlenecks  
*J. Marathe, F. Mueller, B. du Supinski (INCSU, LLNL)*

**10:50 am** A NUCA Substrate for Flexible CMP Cache Sharing  
*J. Huh, C. Kim, H. Shafi, L. Zhang, D. Burger, S. Keckler*

#### 11:10 am Coffee Break

#### Session 2: Value

**11:25 am** Fast Branch Misprediction Recovery in  
Out-of-order Superscalar Processors  
*P. Zhou, S. Onder, S. Carr (MTU)*

**11:45 am** Tornado Warning: the Perils of Selective  
Replay in Multithreaded Processors  
*Y. Liu, A. Shayesteh, G. Memik, G. Reinman*

**12:05 pm** An Asymmetric Clustered Processor  
based on Value Content  
*R. Gonzalez, A. Cristal, A. Veidenbaum, M. Pericas,  
M. Valero (UPC, UCI)*

**12:25 am** A Heterogeneously Segmented Cache  
Architecture for a Packet Forwarding Engine  
*K. Rajan, R. Govindarajan (IIS)*

#### 12:45 - 2:00 pm Lunch

#### Session 3: Sampling

**2:00 pm** Low-Overhead Call Path Profiling of  
Unmodified, Optimized Code  
*N. Froyd, J. Mellor-Crummey, R. Fowler (Rice Univ.)*

**2:20 pm** Design of a Next Generation Sampling  
Service for Large Scale Data Analysis Applications  
*H. Wang, S. Tatikonda, A. Ghoting, G. Buehrer,  
S. Parthasarathy, T. Kurc, J. Saltz (Ohio State Univ.)*

**2:40 pm** Online Performance Analysis by Statistical  
Sampling of Microprocessor Performance Counters  
*R. Azimi, M. Stumm, R. Wisniewski (Univ. of Toronto)*

**3:00 pm** Improved Automatic Testcase Synthesis for  
Performance Model Validation  
*R. H. Bell, L. K. John (U. Texas - Austin)*

#### 3:20 pm Tea Break

#### Session 4: Compilers 1

**3:35 pm** Automatic Thread Distribution For  
Nested Parallelism In OpenMP  
*A. Duran, M. Gonzalez, J. Corbalan, X. Martorell,  
E. Ayguade, J. Labarta, R. Silvera (Tech. Univ. of  
Catalonia)*

**3:55 pm** Lightweight Reference Affinity Analysis  
*X. Shen, Y. Gao, C. Ding, R. Archambault  
(U. Rochester, IBM Toronto Lab)*

**4:15 pm** Think Globally, Search Locally  
*K. Yotov, K. Pingali, P. Stodghill (Cornell Univ.)*

**4:35 pm** Facilitating the Search for Compositions  
of Program Transformations  
*A. Cohen, S. Girbil, M. Gonzalez-Sigler,  
David Parello, Olivier Temam, Nicolas Vasilache  
(Alchemy Group)*

#### Monday Evening

**5:05 pm** Dinner (on your own)

### Tuesday, June 21, 2005

#### Session 5: Compilers II

**8:30 am** Generating New General Compiler  
Optimization Settings  
*M. Haneda, P.M.W. Knijnenburg, H.A.G. Wijshoff (Leiden  
Univ.)*

**8:50 am** An Integrated Simdization Framework Using Virtual  
Vectors  
*P. Wu, A. Eichenberger, A. Wang, P. Zhao (IBM)*

**9:10 am** Tasking with Out-of-Order Spawn in TLS Chip Multi-  
processors: Microarchitecture and Compilation  
*J. Renau, J. Tuck, W. Liu, L. Ceze, K. Strauss, J. Torrellas (U.  
of Illinois)*

**9:30 am** Towards Automatic Translation of OpenMP to MPI  
*Ayon Basumallik, Rudolf Eigenmann (Purdue)*

#### 9:50 am Coffee Break

#### Session 6: Threads

**10:05 am** TAPE: Transactional Application Profiling Environ-  
ment  
*H. Chafi, A. McDonald, C. Cao Minh, J. W. Chung, Brian D.  
Carlstrom, L. Hammond, C. Kozyrakis, K. Olukotun (Stanford)*

**10:25 am** Low Power, Low Complexity Instruction Issue using  
Compiler Assistance  
*M. Valluri, L. John, K. McKinley (UT Austin)*

**10:45 am** Thread-Level Speculation on a CMP Can Be En-  
ergy Efficient  
*J. Renau, K. Strauss, L. Ceze, W. Liu, S. Sarangi, J. Tuck, J.  
Torrellas (UCSC, U. of Illinois)*

**11:05 am** Power-aware Resource Allocation in High-End Sys-  
tems via Online Simulation  
*B. Lawson, E. Smirni (U. of Richmond, College of William and  
Mary)*

#### 11:25 am Coffee Break

#### Session 7: Machines

**11:40 pm** The Architecture of the HP Superdome Shared-  
Memory Multiprocessors  
*G. Gostin, J. Collard, K. Collins (HP)*

**12:00 pm** Scaling Physics and Material Science  
Applications on a Massively Parallel Blue Gene/L System  
*G. Almasi, G. Bhanot, A. Gara, M. Gupta, J. Sexton, B.  
Walkup, V. V. Bulatov, A. W. Cook, B. R. de Supinski, J. A.  
Greenough, F. Gygi, A. Kubota, S. Louis, F. H. Streitz, R.  
Yates, C. Archer, J. Moreira (IBM, LLNL)*

**12:20 pm** Optimization of MPI Collective Communication on BlueGene/L Systems

*G. Almasi, C. J. Archer, C. Chris Erway, P. Heidelberger, X. Martorell, J. E. Moreira, B. Steinmacher-Burow, Y. Zheng (IBM)*

**12:40 pm Lunch**

**Tuesday Afternoon (June 21)**

**PMUA Workshop: Workshop in programming models for HPCS ultra-scale applications**  
(Stata Center: 32 Vassar Street, 32-123)

**2:00 pm** HPCS Workshop and Sessions

**3:30 pm** Break

**3:45 pm** HPCS Workshop and Sessions

**5:30 pm** Relaxation (on your own)

**6:00 pm** Reception (Stata Center - 4th floor, R&D Space)

**7:00 pm** Banquet (Stata Center - 4th floor, R&D Space)

**Wednesday, June 22, 2005**

**8:30 am** Keynote

**David E. Shaw** (D. E. Shaw)

New Architectures for a New Biology

**9:30 am Coffee Break**

**Session 8: Distributed Systems**

**9:50 am** Transparent Caching with Strong Consistency in Dynamic Content Web Sites

*C. Amza, G. Soundararajan, E. Cecchet (U. Toronto, INRIA)*

**10:10 am** Disk Layout Optimization for Reducing Energy Consumption

*S. W. Son, G. Chen, M. Kandemir (PSU)*

**10:30 am** Continuous Replica Placement Schemes in Distributed Systems

*T. Loukopoulos, P. Lampsas, I. Ahmad (HKUST, U. Thessaly, U. Texas)*

**10:50 am** A Performance-Conserving Approach for Reducing Peak Power Consumption in Server Systems

*W. Felter, K. Rajamani, C. Rusu, T. Keller (IBM)*

**11:10 am Coffee Break**

**Session 9: Operating Systems**

**11:25 am** System Noise, OS Clock Ticks, and Fine-Grained Parallel Applications

*D. Tsafir, Y. Etsion, D. G. Feitelson, S. Kirkpatrick (The Hebrew Univ.)*

**11:45 am** Another approach to backfilled jobs: applying Virtual Malleability to expired windows

*G. Utrera, J. Corbalan, J. Labarta (UPC)*

**12:05 pm** High Performance Support of Parallel Virtual File System (PVFS2) over Quadrics

*W. Yu, S. Liang, D. K. Panda (Ohio State Univ.)*

**12:25 pm** The Implications of Working Set Analysis on Supercomputing Memory Hierarchy Design

*R. C. Murphy, A. Rodrigues, P. M. Kogge, Keith Underwood (UND)*

**12:45 pm Lunch**

**Session 10: Applications**

**2:00 pm** Improving the Computational Intensity of Unstructured Mesh Applications

*B. S. White, S. A. McKee, B. R. de Supinski, B. Miller, D. Quinlan, M. Schulz (Cornell, LLNL)*

**2:20 pm** Parallel Sparse LU Factorization on Second-class Message Passing Platforms

*K. Shen (U. Rochester)*

**2:40 pm** Cache Oblivious Stencil Computations

*M. Frigo, V. Strumpen (IBM)*

**3:00 pm** Multigrain Parallel Delaunay Mesh Generation: Challenges and Opportunities for Multithreaded Architectures

*C. D. Antonopoulos, X. Ding, A. Chernikov, F. Blagojevic, D. Nikolopoulos, N. Chrisochoides (College of William and Mary)*

**3:20 pm Tea Break**

**Session 11: System-Wide Issues**

**3:35 pm** What is Worth Learning from Parallel Workloads? A User and Session Based Analysis

*J. Zilber, O. Amit, D. Talby (Hadassah College, Hebrew Univ.)*

**3:55 pm** affinity-on-next-touch: Increasing the Performance of an Industrial PDE Solver on a cc-NUMA System

*H. Lof, S. Holmgren (Uppsala Univ.)*

**4:15 pm** Automatic Generation and Tuning of MPI Collective Communication Routines

*A. Faraj, X. Yuan (Florida State Univ.)*

**4:35 pm Closing Remarks**

**4:45 pm End of Conference**

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## Proceedings of The 19th ACM International Conference on Supercomputing

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**June 20 - 22, 2005**  
**(Workshop Tutorials - June 19th)**

The Cambridge Marriott (Kendall Square)  
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